CLAIMS:

Sub C1

1. A method of running an algorithm wherein the algorithm comprises a first function and a second function, the method comprising the following steps:

a first step of requesting an algorithm resource by the algorithm to provide a plurality of output quality levels,

a second step of determining that the first function provides a first plurality of quality levels and the second function provides a second plurality of quality levels,

a third step of allocating a budget to the algorithm to enable operating the algorithm at a output quality level, said output quality level being one of the plurality of output quality levels,

a fourth step of assigning a first quality level of the first plurality of quality levels to the first function and of assigning a second quality level of the second plurality of quality levels to the second function.

2. A method of running an algorithm according to claim 1, further comprising a fifth step of determining that the first function, while providing the first quality level, can be operated at a plurality of levels of complexity.

3. A method of running an algorithm according to claim 1, further comprising the following steps:

a sixth step of operating the algorithm at the output quality level.

a seventh step of operating the first function at the first quality level while consuming a first amount of resources by the first function and operating the second function at the second quality level while consuming a second amount of resources by the second function.

4. A method of running an algorithm according to claim 3, further comprising an eighth step of operating the first function at a least complex level of the plurality of levels of complexity.

5. A method of running an algorithm according to claim 1, wherein the allocated budget is substantially equal to the requested algorithm resource.

6. A method of running an algorithm according to claim 3, wherein the first amount of resources in addition to the second amount of resources is substantially equal to the allocated budget.

7. A method of running an algorithm according to claim 1, further comprising a ninth step of determining a hardware platform operating said method to determine the algorithm resource and the plurality of output quality levels.

8. A method of running an algorithm according to claim 1, further comprising an tenth step of determining a software platform operating said method to determine the algorithm resource and the plurality of output quality levels.

9. A method for operating a programmable processing device to reduce distortion in an outputted signal, the method comprising the following steps:

a first step of providing data indicative of a plurality of operational states (202), each of said states (202) being associated with at least one of a plurality of operational modes (1002, 1004, 1006, 1008) of said device, a complexity of operations (C) and a distortion level (D);

a second step of selecting one of said states for each of said complexities using said data and based upon said distortion levels;

a third step of determining an operating status of said device; and,

a fourth step of selecting which of said operational modes to operate said device in for each of said complexities responsively to said determined status using said selected states.

10. A method for operating a programmable processing device to reduce distortion in an outputted signal according to claim 9, wherein said selected operational mode for a first determined status is different from said selected operational mode for a second determined status.

11. A method for operating a programmable processing device to reduce distortion in an outputted signal according to claim 9, wherein said second step is based upon minimizing said distortion level for said complexity.

12. A method for operating a programmable processing device to reduce distortion in an outputted signal according to claim 9, wherein said first step comprises using at least one lookup table.

13. A method for operating a programmable processing device to reduce distortion in an outputted signal according to claim 9, wherein said programmable device is a multimedia communications device.

14. A method for operating a programmable processing device to reduce distortion in an outputted signal according to claim 9, wherein said device is an ATSC compliant digital television decoder including at least one IDCT, and each of said modes corresponds to a different mode of operation of said at least one IDCT.

15. A method for operating a programmable processing device to reduce distortion in an outputted signal according to claim 9, wherein said selecting comprises determining which of said modes provides a complexity-distortion characteristic desirable to those of said other modes for performing said task using said available amount of computing resources.

16. A scalable programmable processing device comprising:

at least one scalable application (300') operable in plurality of modes each having a different complexity of operations characteristic;

a QOS resource manager (800) for tracking how much computing resources are available for use by said at least one scalable application (300');

a strategy manager (802) for determining whether said available resources are suitable for operation of said scalable application (300') in a given one of said modes; and,

a local resource control (804) responsive to said strategy manager (802) and for selecting, in response to a determination by said strategy manager (802) that said available resources are not suitable for operation of said at least one application (300') in said given mode to select another of said modes for said at least one application (300');

wherein, said QOS manager (800) and strategy manager (802) are mutually responsive to one another and said at least one scalable application (300') is responsive to said local resource control (804).

17. A scalable programmable processing device according to claim 16, further comprising a memory accessible to said local resource control.

18. A scalable programmable processing device according to claim 17, wherein said memory includes a data being indicative of complexity-distortion characteristics of each of said modes for a plurality of amounts of available system resources.

19. A scalable programmable processing device according to claim 16, wherein said device is an ATSC compliant digital television decoder including at least one IDCT, and each of said modes corresponds to a different mode of operation of said at least one IDCT.

20. A scalable MPEG2 compatible video decoder comprising:

at least one variable length decoder (304');

at least one inverse quantizer (310') coupled to said variable length decoder (300');

at least one inverse discrete cosine transform (312') coupled to said inverse quantizer (310');

at least one motion compensator (306) coupled to said variable length decoder (304');

a summing junction (314) coupled to said inverse discrete cosine transform (312') and motion compensator (306); and,

a controller (804);

wherein at least one of said variable length decoder (304'), inverse quantizer (310'), inverse discrete cosine transform (312') and motion compensator (306) is coupled to said controller and responsive thereto to operate in one of a plurality of modes each having a given complexity characteristic for an acceptable distortion level of an output of said decoder; and, wherein said controller selects said one of said modes based upon said given complexity characteristics.

21. A scalable MPEG2 compatible video decoder according to claim 20, wherein said controller selects said one of said modes further based upon an available amount of computing resources for operating at least one of said variable length decoder (304'), inverse quantizer (310'), inverse discrete cosine transform (312') and motion compensator (306').

22. A scalable MPEG2 compatible video decoder according to claim 20, wherein said at least one inverse discrete cosine transform (312') includes a plurality of inverse discrete cosine transforms (312, 312', 312") which is selectively operable in response to said controller (804).

23. A scalable MPEG2 compatible video decoder according to claim 22, wherein said selectively operated inverse discrete cosine transform (312, 312', 312") implements said selected one of said modes.

24. A scalable MPEG2 compatible video decoder according to claim 23, wherein said complexity-distortion characteristic of said selected one of said modes is more efficient than those of the others of said plurality of modes.

25. A computer program product arranged to perform the method according to any of the claims 1 to 15.

26. A storage device (700) comprising a computer program product according to claim 25.